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WE CLAIM:

1   1.   A circuit arrangement for sampling a logic data signal, comprising:

2   a first timer adapted to time a first time interval;

3   a delay timer coupled to the first timer and adapted to time a delay time interval

4   initiated from the start of the first time interval;

5   a second timer coupled to the delay timer and adapted to time a second time

6   interval initiated at the end of the delay time interval;

7   a coincidence circuit having an input terminal for receiving the logic data signal,

8   an output terminal, and an enable terminal coupled to the second timer, the coincidence

9   circuit adapted to pass a sample of digital event pulses comprising the logic data signal

10 from the input terminal to the output terminal during the second time interval.

1   2.   The circuit arrangement of claim 1, wherein the first timer is a binary count

2   register having N+1 bits, the delay timer is a latch register having N bits, and the binary

3   count register and latch register are coupled to a comparator circuit, and the comparator

4   circuit adapted to initiate the second timer when the value of the binary count register and

5   the value of the latch register are equivalent.

1   3.   The circuit arrangement of claim 2, wherein the delay timer is adapted to pseudo-

2   randomly vary the delay time interval.

1   4.   The circuit arrangement of claim 3, wherein the delay timer is adapted to select the

2   delay time interval from a finite set of discrete times.

1   5.   The circuit arrangement of claim 3, wherein the latch register is a latching shift

2   register.

1   6.   The circuit arrangement of claim 5, further comprising a pseudo-random number

2   generator coupled to the latch register, the pseudo-random number generator having less

3   bits than the latch register and the pseudo-random number generator adapted to seed the

4   latch register.

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1   7.   The circuit arrangement of claim 6, wherein the latching shift register is a round

2   robin latch.

1   8.   The circuit arrangement of claim 7, wherein the second timer is a second binary

2   counter having M+1 bits, M being less than or equal to N.

1   9.   The circuit arrangement of claim 8, wherein the first timer is adapted to time a

2   series of periodic first time intervals.

1   10.   The circuit arrangement of claim 9, wherein the delay timer is adapted to

2   determine and time a new delay time interval for each first time interval in the series of

3   first time intervals.

1   11.   The circuit arrangement of claim 10, further comprising a counting circuit coupled

2   to the output terminal of the coincidence circuit, the counting circuit adapted to

3   accumulate a count of the digital event pulses in the sample.

1   12.   The circuit arrangement of claim 11, wherein the counting circuit is reset

2   responsive to the first timer.

1   13.   A circuit arrangement for sampling a plurality of digital event pulses, comprising:

2   a first timer adapted to time a plurality of base time intervals;

3   a second timer adapted to generate a sampling window signal for a sampling

4   window time interval, the sampling window time interval being a shorter time than any of

5   the base time intervals;

6   a sample window initiate circuit coupled to the first timer and adapted to start the

7   second timer at a pseudo-random time within each of the plurality of base time intervals;

8   and

9   a sampler circuit coupled to the second timer and arranged to receive the plurality

10   of digital event pulses and to pass a sample of digital event pulses responsive to the

11   sampling window signal.

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1 14. The circuit arrangement of claim 13, further comprising a counting circuit coupled

2 to the sampler circuit, the counting circuit adapted to accumulate a count of the sample of

3 digital event pulses.

1 15. The circuit arrangement of claim 14, wherein the counting circuit is a digital

2 counter.

1 16. The circuit arrangement of claim 14, wherein the counting circuit further

2 comprises a capacitor coupled through a transistor to a constant current source, the

3 transistor being responsive to each of the digital event pulses to pass a substantially fixed

4 amount of charge from the constant current source to the capacitor.

1 17. The circuit arrangement of claim 15, wherein the first timer is a binary counter

2 having $N+1$ bits, and the second timer is a binary counter having $M+1$ bits, M being less

3 than or equal to N.

1 18. The circuit arrangement of claim 17, wherein the first and second timers are

2 adapted to count clock cycles, and the pseudo-random time being a discrete binary value

3 of first timer.

1 19. The circuit arrangement of claim 18, wherein the sampling window initiate circuit

2 comprises a pseudo-random number generator having K bits coupled to a shift register

3 having N bits, the shift register arranged to receive and shift binary pseudo-random

4 numbers from the pseudo-random number generator to form N bit pseudo-random

5 numbers, whereby K is less than or equal to N.

1 20. The circuit arrangement of claim 19, wherein the shift register is a round robin

2 latch.

1 21. The circuit arrangement of claim 20, wherein the overflow bit of the first timer is

2 coupled to the counting circuit, the counting circuit adapted to reset responsive to the

3 overflow bit of the first timer.

1   22.   A method for sampling a logic data signal, comprising:

2   receiving a plurality of digital event pulses characterizing the logic data signal

3   during each of a series of base time intervals;

4   applying a sampling window signal for a sample window time interval beginning

5   at a pseudo-random time during each of a series of base time intervals;

6   selecting a subset of digital event pulses during application of the sampling

7   window signal; and

8   accumulating a count of the subset digital event pulses.

1   23.   The method of claim 22, further comprising:

2   timing each base time interval with a base time binary counter, the base time

3   binary counter adapted to count clock cycles; and

4   timing the sample window time interval with a sample window binary counter, the

5   sample window binary counter adapted to count clock cycles.

1   24.   The method of claim 23, further comprising:

2   seeding a round robin latch with a pseudo-random number generator, the round

3   robin latch having a length of N bits, the base time counter having a length of $N+1$ bits,

4   and the pseudo-random number generator having fewer bits than the round robin latch;

5   shifting round robin latch bit values and populating all bits of the round robin

6   latch;

7   forming an N bit pseudo-random number in the round robin latch; and

8   initiating timing of the sample window time interval when a value of the base time

9   binary counter is equivalent to a value of the round robin latch.

1   25.   The method of claim 24, further comprising resetting the count of the subset of

2   digital event pulses accumulated at the end of each base time interval.

1   26.   A circuit arrangement to sample a logic data signal, comprising:

2   means for receiving a plurality of digital event pulses characterizing the logic data

3   signal during each of a series of base time intervals;

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4   means for applying a sampling window signal for a sample window time interval

5   beginning at a pseudo-random time during each of a series of base time intervals;

6   means for selecting a subset of digital event pulses during application of the

7   sampling window signal; and

8   means for accumulating a count of the subset digital event pulses.